SAVITRIBAI PHULE PUNE UNIVERSITY, B.E.(2012 COURSE) EXAMINATION,OCT/NOV 2017

BRANCH:71-B.E. (2012 PAT.)(ELECTRONICS &TELECOMUNICATION)

DATE : 16 JAN 2018 CENTRE: MODERN EDU.SOC.'S COLL.OF ENGINEERING, PUNE

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323132 SHAH NISHIT VIJAYKUMAR KALPANA ,71211429H ,MESP ,B120323132

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	47	63	P	
404182	COMPUTER NETWORKS	PP	70	28	13	37	50	P	
404183	MICROWAVE ENGINEERING	PP	70	28	26	48	74	P	
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	15	29	44	P	C
404185C	PLCS AND AUTOMATION	PP	70	28	22	34	56	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			35	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P	C
404188	PROJECT PHASE I	OR	50	20			45	P	C

SEM.:2

404189	MOBILE COMMUNICATION	PP	70	28	09	32	41	P	C
404190	BROADBAND COMMUNICATION SYS.	PP	70	28	19	35	54	P	C
404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	14	28$	42	P	C
404192D	WIRELESS NETWORKS	PP	70	28	20	38	58	P	C
404193	LAB PRACTICE III(MC & BCS)	TW	50	20			29	P	C
404193	LAB PRACTICE III(MC & BCS)	OR	50	20			30	P	C
404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			39	P	C
404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			37	P	C
404195	PROJECT PHASE II	TW	100	40			92	P	C
404195	PROJECT PHASE II	PR	50	20			40	P	C

GRAND TOTAL = 942/1500 , RESULT:FIRST CLASS [$ O.1]

B120323113 UZAIR CHOWDHARY MEHER ,71211484L ,MESP ,B120323113

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	05	--	F
404182	COMPUTER NETWORKS	PP	70	28	14	AA	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	25	AA	--	F
404184C	SOFTWARE DEFINED RADIO	PP	70	28	21	AA	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	16	AA	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323045 HARALE MUKESH BALAJI JANABAI ,71211240F ,MESP ,B120323045

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	09	29	--	F
404182	COMPUTER NETWORKS	PP	70	28	08	16	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	04	28	--	F
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	11	28	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	12	32	44	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			28	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			25	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			20	P
404188	PROJECT PHASE I	OR	50	20			20	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323099 SHAIKH MATEEN WAHID RUKSAR ,71223187M ,MESP ,B120323099

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	10	17	--	F
404182	COMPUTER NETWORKS	PP	70	28	13	14	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	16	34	50	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	12	23	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	18	24	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			AA	F
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			AA	F
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			24	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			05	F
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323012 BHAGWAT PRAJAKTA SARJERAO SHAKUNTALA ,71312320G ,MESP ,B120323012

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	30	43	P
404182	COMPUTER NETWORKS	PP	70	28	16	08	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	09	17	--	F
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	18	48	66	P
404185C	PLCS AND AUTOMATION	PP	70	28	19	37	56	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			33	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			36	P

FIRST SEM TOTAL = --/750

B120323124 CHOUDHARY YOGESH KUMARNARAYAN SULOCHANA ,71312360F ,MESP ,B120323124

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	05	35$	40	P	C
404182	COMPUTER NETWORKS	PP	70	28	19	38	57	P	
404183	MICROWAVE ENGINEERING	PP	70	28	25	31	56	P	
404184C	SOFTWARE DEFINED RADIO	PP	70	28	06	44	50	P	C
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	06	38	44	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			22	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			25	P	C
404188	PROJECT PHASE I	OR	50	20			33	P	C

SEM.:2

404189	MOBILE COMMUNICATION	PP	70	28	14	31	45	P	
404190	BROADBAND COMMUNICATION SYS.	PP	70	28	20	30	50	P	C
404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	09	39	48	P	C
404192B	NANO ELECTRONICS & MEMS	PP	70	28	14	31	45	P	C
404193	LAB PRACTICE III(MC & BCS)	TW	50	20			22	P	C
404193	LAB PRACTICE III(MC & BCS)	OR	50	20			24	P	C
404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			24	P	C
404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			20	P	C
404195	PROJECT PHASE II	TW	100	40			82	P	C
404195	PROJECT PHASE II	PR	50	20			38	P	C

GRAND TOTAL = 793/1500 , RESULT:SECOND CLASS [$ O.1]

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323075 MULANGE SUSHIL SUDHAKAR SUNITA ,71312521H ,MESP ,B120323075

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	10	01	--	F
404182	COMPUTER NETWORKS	PP	70	28	11	13	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	07	07	--	F
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	08	08	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	14	11	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			35	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			20	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			07	F
404188	PROJECT PHASE I	OR	50	20			37	P

FIRST SEM TOTAL = --/750

B120323134 SUSHMITA SADASHIV DONGARE SNEHAL ,71312630C ,MESP ,B120323134

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	33	49	P	C
404182	COMPUTER NETWORKS	PP	70	28	15	28	43	P	C
404183	MICROWAVE ENGINEERING	PP	70	28	18	30	48	P	
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	37	59	P	C
404185C	PLCS AND AUTOMATION	PP	70	28	25	38	63	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P	C
404188	PROJECT PHASE I	OR	50	20			44	P	C

SEM.:2

404189	MOBILE COMMUNICATION	PP	70	28	12	31	43	P	
404190	BROADBAND COMMUNICATION SYS.	PP	70	28	11	29$	40	P	C
404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	16	38	54	P	C
404192B	NANO ELECTRONICS & MEMS	PP	70	28	14	40	54	P	C
404193	LAB PRACTICE III(MC & BCS)	TW	50	20			38	P	C
404193	LAB PRACTICE III(MC & BCS)	OR	50	20			33	P	C
404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			42	P	C
404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			40	P	C
404195	PROJECT PHASE II	TW	100	40			96	P	C
404195	PROJECT PHASE II	PR	50	20			46	P	C

GRAND TOTAL = 951/1500 , RESULT:FIRST CLASS [$ O.1]

B120323087 PODDAR ABHIJIT PRAKASH MEENA ,71312658C ,MESP ,B120323087

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	10	18	--	F
404182	COMPUTER NETWORKS	PP	70	28	09	08	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	12	36	48	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	06	10	--	F
404185C	PLCS AND AUTOMATION	PP	70	28	16	09	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			22	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			28	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			21	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			08	F
404188	PROJECT PHASE I	OR	50	20			20	P

FIRST SEM TOTAL = --/750

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B120323126 GODSE SANKET SOPAN RANGANA ,71312408D ,MESP ,B120323126

SEM.:1									SEM.:2								
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	30	45	P C	404189	MOBILE COMMUNICATION	PP	70	28	05	36	41	P C
404182	COMPUTER NETWORKS	PP	70	28	04	41	45	P C	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	18	35	53	P
404183	MICROWAVE ENGINEERING	PP	70	28	04	39	43	P C	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	12	47	59	P C
404184C	SOFTWARE DEFINED RADIO	PP	70	28	04	42	46	P C	404192B	NANO ELECTRONICS & MEMS	PP	70	28	20	45	65	P C
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	21	52	73	P C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			21	P C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			27	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			32	P C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			40	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			28	P C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			41	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			28	P C	404195	PROJECT PHASE II	TW	100	40			85	P C
404188	PROJECT PHASE I	OR	50	20			39	P C	404195	PROJECT PHASE II	PR	50	20			33	P C

GRAND TOTAL = 884/1500 , RESULT:HIGHER SECOND CLASS

B120323123 CHHATRE SHIVANAND LAXMANRAO CHANDRAKALABAI ,71312356H ,MESP ,B120323123

SEM.:1									SEM.:2								
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	28	40	P C	404189	MOBILE COMMUNICATION	PP	70	28	13	28$	41	P C
404182	COMPUTER NETWORKS	PP	70	28	14	28	42	P C	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	20	28	48	P C
404183	MICROWAVE ENGINEERING	PP	70	28	27	30	57	P	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	10	34	44	P C
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	11	25	--	F	404192B	NANO ELECTRONICS & MEMS	PP	70	28	22	43	65	P C
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	13	29	42	P C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			22	P C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			34	P C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			22	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			27	P C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			35	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			23	P C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			30	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			20	P C	404195	PROJECT PHASE II	TW	100	40			79	P C
404188	PROJECT PHASE I	OR	50	20			31	P C	404195	PROJECT PHASE II	PR	50	20			36	P C

GRAND TOTAL = --/1500 , RESULT:FAILS [$ O.1]

B120323121 BHOR MAYUR PANDURANG VANDANA ,71412238G ,MESP ,B120323121

SEM.:1									SEM.:2								
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	09	39	48	P C	404189	MOBILE COMMUNICATION	PP	70	28	09	33	42	P C
404182	COMPUTER NETWORKS	PP	70	28	14	31	45	P C	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	09	43	52	P C
404183	MICROWAVE ENGINEERING	PP	70	28	11	29$	40	P C	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	12	32	44	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	20	40	60	P C	404192D	WIRELESS NETWORKS	PP	70	28	13	39	52	P C
404185C	PLCS AND AUTOMATION	PP	70	28	20	32	52	P C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			30	P C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			32	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			34	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			30	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			37	P C	404195	PROJECT PHASE II	TW	100	40			73	P C
404188	PROJECT PHASE I	OR	50	20			35	P C	404195	PROJECT PHASE II	PR	50	20			32	P C

GRAND TOTAL = 841/1500 , RESULT:HIGHER SECOND CLASS [$ O.1]

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323057 KAMBLE PANKAJ VILAS JAYSHREE ,71412356M ,MESP ,B120323057

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	44	58	P
404182	COMPUTER NETWORKS	PP	70	28	14	29	43	P
404183	MICROWAVE ENGINEERING	PP	70	28	16	52	68	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	13	37	50	P
404185C	PLCS AND AUTOMATION	PP	70	28	16	39	55	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			28	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			06	F
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323112 UNDIRWADE NIKHIL MILIND MAYA ,71412586F ,MESP ,B120323112

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	30	44	P
404182	COMPUTER NETWORKS	PP	70	28	14	25	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	18	33	51	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	16	21	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	20	36	56	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			43	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			43	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = --/750

B120323136 VASEKAR TEJAS SHYAMKANT SHAILAJA ,71412589L ,MESP ,B120323136

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	32	45	P	C
404182	COMPUTER NETWORKS	PP	70	28	20	32	52	P	
404183	MICROWAVE ENGINEERING	PP	70	28	20	29	49	P	C
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	19	44	63	P	C
404185C	PLCS AND AUTOMATION	PP	70	28	18	50	68	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P	C
404188	PROJECT PHASE I	OR	50	20			46	P	C

SEM.:2

404189	MOBILE COMMUNICATION	PP	70	28	16	28	44	P	
404190	BROADBAND COMMUNICATION SYS.	PP	70	28	16	32	48	P	C
404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	19	36	55	P	C
404192B	NANO ELECTRONICS & MEMS	PP	70	28	18	41	59	P	C
404193	LAB PRACTICE III(MC & BCS)	TW	50	20			25	P	C
404193	LAB PRACTICE III(MC & BCS)	OR	50	20			33	P	C
404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			41	P	C
404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			40	P	C
404195	PROJECT PHASE II	TW	100	40			94	P	C
404195	PROJECT PHASE II	PR	50	20			45	P	C

GRAND TOTAL = 956/1500 , RESULT:FIRST CLASS

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323035 GAWANKAR SARVESH BHALCHANDRA VAISHALI ,71412294H ,MESP ,B120323035

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	02	08	--	F
404182	COMPUTER NETWORKS	PP	70	28	08	01	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	14	AA	--	F
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	08	AA	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	07	AA	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			AA	F
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			AA	F
404188	PROJECT PHASE I	OR	50	20			36	P

FIRST SEM TOTAL = --/750

B120323100 SHINDE ASHWINI SANGITA ,71412543B ,MESP ,B120323100

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	29	43	P
404182	COMPUTER NETWORKS	PP	70	28	12	25	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	11	32	43	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	14	51	65	P
404185C	PLCS AND AUTOMATION	PP	70	28	21	04	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			33	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323103 SOMAWAR PRANAV NARESH SHUBHANGI ,71412555F ,MESP ,B120323103

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	16	--	F
404182	COMPUTER NETWORKS	PP	70	28	10	20	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	15	35	50	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	16	35	51	P
404185C	PLCS AND AUTOMATION	PP	70	28	24	40	64	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			42	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323072 MARSALE ADITYA PRAKASH ARUNA ,71412412F ,MESP ,B120323072

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	09	18	--	F
404182	COMPUTER NETWORKS	PP	70	28	14	35	49	P
404183	MICROWAVE ENGINEERING	PP	70	28	10	39	49	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	14	37	51	P
404185C	PLCS AND AUTOMATION	PP	70	28	17	29	46	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			32	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323130 PAL ADITYA RAJU ANURADHA ,71412446L ,MESP ,B120323130

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	31	42	P
404182	COMPUTER NETWORKS	PP	70	28	10	30$	40	P
404183	MICROWAVE ENGINEERING	PP	70	28	20	28	48	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	13	28	41	P C
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	19	30	49	P C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P C
404188	PROJECT PHASE I	OR	50	20			43	P C

SEM.:2

404189	MOBILE COMMUNICATION	PP	70	28	17	34	51	P C
404190	BROADBAND COMMUNICATION SYS.	PP	70	28	19	43	62	P C
404191D	SOFT COMPUTING	PP	70	28	17	34	51	P C
404192D	WIRELESS NETWORKS	PP	70	28	10	48	58	P C
404193	LAB PRACTICE III(MC & BCS)	TW	50	20			28	P C
404193	LAB PRACTICE III(MC & BCS)	OR	50	20			35	P C
404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			33	P C
404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			35	P C
404195	PROJECT PHASE II	TW	100	40			88	P C
404195	PROJECT PHASE II	PR	50	20			44	P C

GRAND TOTAL = 895/1500 , RESULT:HIGHER SECOND CLASS [$ O.1]

B120323133 SHINDE DINESH PARMESHWAR ASHABAI ,71412544L ,MESP ,B120323133

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	10	30$	40	P C
404182	COMPUTER NETWORKS	PP	70	28	20	29	49	P
404183	MICROWAVE ENGINEERING	PP	70	28	11	31	42	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	18	35	53	P C
404185C	PLCS AND AUTOMATION	PP	70	28	21	AA	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			36	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P C
404188	PROJECT PHASE I	OR	50	20			34	P C

SEM.:2

404189	MOBILE COMMUNICATION	PP	70	28	18	33	51	P C
404190	BROADBAND COMMUNICATION SYS.	PP	70	28	11	29$	40	P C
404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	09	10	--	F
404192D	WIRELESS NETWORKS	PP	70	28	16	36	52	P
404193	LAB PRACTICE III(MC & BCS)	TW	50	20			25	P C
404193	LAB PRACTICE III(MC & BCS)	OR	50	20			29	P C
404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			34	P C
404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			35	P C
404195	PROJECT PHASE II	TW	100	40			75	P C
404195	PROJECT PHASE II	PR	50	20			35	P C

GRAND TOTAL = --/1500 , RESULT:FAILS [$ O.1]

RESULT RESERVED FOR BACKLOGS.

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323135 THOMBARE MAYURESH SATISH NILEEMA ,71412575L ,MESP ,B120323135

SEM.:1									SEM.:2							
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	29$	40	P	404189	MOBILE COMMUNICATION	PP	70	28	09	31$	40	P C
404182	COMPUTER NETWORKS	PP	70	28	17	34	51	P	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	16	42	58	P C
404183	MICROWAVE ENGINEERING	PP	70	28	19	22	--	F	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	18	47	65	P C
404184C	SOFTWARE DEFINED RADIO	PP	70	28	02	56	58	P C	404192B	NANO ELECTRONICS & MEMS	PP	70	28	20	45	65	P C
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	11	37	48	P C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			24	P C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			34	P C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			26	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			33	P C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			38	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			28	P C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			36	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P C	404195	PROJECT PHASE II	TW	100	40			91	P C
404188	PROJECT PHASE I	OR	50	20			39	P C	404195	PROJECT PHASE II	PR	50	20			42	P C

GRAND TOTAL = --/1500 , RESULT:FAILS [$ O.1]

B120323137 VIJAY M MUNJE KASHIBAI ,71412592L ,MESP ,B120323137

SEM.:1									SEM.:2							
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	08	36	44	P C	404189	MOBILE COMMUNICATION	PP	70	28	11	29$	40	P C
404182	COMPUTER NETWORKS	PP	70	28	14	32	46	P	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	16	37	53	P
404183	MICROWAVE ENGINEERING	PP	70	28	08	32$	40	P C	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	09	31$	40	P C
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	10	31	41	P C	404192D	WIRELESS NETWORKS	PP	70	28	14	45	59	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	12	28$	40	P C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			25	P C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			24	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			34	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			33	P C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			35	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			29	P C	404195	PROJECT PHASE II	TW	100	40			92	P C
404188	PROJECT PHASE I	OR	50	20			38	P C	404195	PROJECT PHASE II	PR	50	20			43	P C

GRAND TOTAL = 822/1500 , RESULT:SECOND CLASS [$ O.1]

B120323125 DIVATE KIRAN RAMESH KESHAR ,71412276K ,MESP ,B120323125

SEM.:1									SEM.:2							
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	24	--	F	404189	MOBILE COMMUNICATION	PP	70	28	04	36$	40	P
404182	COMPUTER NETWORKS	PP	70	28	11	29	40	P C	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	16	33	49	P
404183	MICROWAVE ENGINEERING	PP	70	28	10	24	--	F	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	03	16	--	F
404184C	SOFTWARE DEFINED RADIO	PP	70	28	15	41	56	P	404192D	WIRELESS NETWORKS	PP	70	28	08	38	46	P
404185C	PLCS AND AUTOMATION	PP	70	28	17	40	57	P C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			25	P C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			27	P C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			39	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			35	P C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			33	P C	404195	PROJECT PHASE II	TW	100	40			90	P C
404188	PROJECT PHASE I	OR	50	20			38	P C	404195	PROJECT PHASE II	PR	50	20			42	P C

GRAND TOTAL = --/1500 , RESULT:FAILS [$ O.1]

RESULT RESERVED FOR BACKLOGS.

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323101 SHINDE PRAJAKTA RAMCHANDRA SUJATA ,71412546G ,MESP ,B120323101

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	05	--	F
404182	COMPUTER NETWORKS	PP	70	28	15	13	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	05	17	--	F
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	18	26	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	16	44	60	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			27	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323030 GAIKWAD AKSHAY BHIVA MANGAL ,71412286G ,MESP ,B120323030

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	25	--	F
404182	COMPUTER NETWORKS	PP	70	28	13	38	51	P
404183	MICROWAVE ENGINEERING	PP	70	28	13	32	45	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	14	43	57	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	13	49	62	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			22	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			08	F
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323014 BHIUNGADE SWAPNIL MADHUKAR SWATI ,71637962H ,MESP ,B120323014

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	33	44	P
404182	COMPUTER NETWORKS	PP	70	28	04	25	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	09	35	44	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	16	33	49	P
404185C	PLCS AND AUTOMATION	PP	70	28	24	31	55	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			33	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323054 KALE DIPALI DNYANESHWAR NANDA ,71637986E ,MESP ,B120323054

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	38	53	P
404182	COMPUTER NETWORKS	PP	70	28	22	47	69	P
404183	MICROWAVE ENGINEERING	PP	70	28	18	47	65	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	24	43	67	P
404185C	PLCS AND AUTOMATION	PP	70	28	22	40	62	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 506/750

B120323066 KSHIRSAGAR SAYALI UTTAM SULBHA ,71637995D ,MESP ,B120323066

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	22	50	72	P
404182	COMPUTER NETWORKS	PP	70	28	23	32	55	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	61	76	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	20	46	66	P
404185C	PLCS AND AUTOMATION	PP	70	28	20	43	63	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 525/750

B120323073 MHASKE POOJA BALASO CHHAYA ,71638001D ,MESP ,B120323073

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	41	52	P
404182	COMPUTER NETWORKS	PP	70	28	19	36	55	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	53	70	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	12	40	52	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	14	33	47	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			31	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			04	F
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323021 DEORE TWINKLE SURESH REKHA ,71637964D ,MESP ,B120323021

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	20	--	F
404182	COMPUTER NETWORKS	PP	70	28	07	39	46	P
404183	MICROWAVE ENGINEERING	PP	70	28	13	34	47	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	17	34	51	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	14	22	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			33	P
404188	PROJECT PHASE I	OR	50	20			37	P

FIRST SEM TOTAL = --/750

B120323043 GUNJAL RASIKA RAJENDRA SANDHYA ,71637980F ,MESP ,B120323043

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	56	74	P
404182	COMPUTER NETWORKS	PP	70	28	22	42	64	P
404183	MICROWAVE ENGINEERING	PP	70	28	21	48	69	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	27	50	77	P
404185C	PLCS AND AUTOMATION	PP	70	28	27	40	67	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			43	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P
404188	PROJECT PHASE I	OR	50	20			36	P

FIRST SEM TOTAL = 545/750

B120323047 JADHAV KAJAL VASANT SHAKUNTALA ,71637982B ,MESP ,B120323047

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	40	54	P
404182	COMPUTER NETWORKS	PP	70	28	18	36	54	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	41	56	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	48	70	P
404185C	PLCS AND AUTOMATION	PP	70	28	22	36	58	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 474/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323071 MANE PRACHI HEMANT UMA ,71638000F ,MESP ,B120323071

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	47	64	P
404182	COMPUTER NETWORKS	PP	70	28	20	40	60	P
404183	MICROWAVE ENGINEERING	PP	70	28	14	56	70	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	20	37	57	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	17	36	53	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 487/750

B120323078 NIBRAD PRAJAKTARANI VINOD MANGALA ,71638006E ,MESP ,B120323078

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	09	35	44	P
404182	COMPUTER NETWORKS	PP	70	28	09	39	48	P
404183	MICROWAVE ENGINEERING	PP	70	28	09	39	48	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	08	43	51	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	10	28	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			22	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = --/750

B120323091 SALGAR POOJA MALLINATH SUNANDA ,71638016B ,MESP ,B120323091

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	18	--	F
404182	COMPUTER NETWORKS	PP	70	28	07	20	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	13	30	43	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	19	22	--	F
404185C	PLCS AND AUTOMATION	PP	70	28	12	26	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			37	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323097 SAWANT HARSHAWARDHAN TULSHIRAM VAIJAYANTA ,71638019G ,MESP ,B120323097

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	20	--	F
404182	COMPUTER NETWORKS	PP	70	28	19	28	47	P
404183	MICROWAVE ENGINEERING	PP	70	28	12	32	44	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	18	29	47	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	09	45	54	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = --/750

B120323109 THORAT ARTI KASHINATH ALKA ,71638024C ,MESP ,B120323109

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	21	45	66	P
404182	COMPUTER NETWORKS	PP	70	28	22	39	61	P
404183	MICROWAVE ENGINEERING	PP	70	28	25	61	86	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	28	50	78	P
404185C	PLCS AND AUTOMATION	PP	70	28	29	62	91	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			42	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 581/750

B120323116 WAKPANJAR VICKY SURESHRAO MEENA ,71638028F ,MESP ,B120323116

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	28	42	P
404182	COMPUTER NETWORKS	PP	70	28	14	25	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	14	37	51	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	15	33	48	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	37	60	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			34	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			32	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			21	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323118 YADAV SWATI BHANUDAS SANGITA ,71638029D ,MESP ,B120323118

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	07	23	--	F
404182	COMPUTER NETWORKS	PP	70	28	19	29	48	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	35	50	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	47	69	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	24	37	61	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			21	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = --/750

B120323002 ADHALGE RUPALI RAMESH ALKA ,71637956C ,MESP ,B120323002

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	38	50	P
404182	COMPUTER NETWORKS	PP	70	28	17	41	58	P
404183	MICROWAVE ENGINEERING	PP	70	28	16	31	47	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	16	42	58	P
404185C	PLCS AND AUTOMATION	PP	70	28	18	31	49	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 438/750

B120323026 DHAGE ASHWINI AMBERNATH SUNANDA ,71637967J ,MESP ,B120323026

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	33	48	P
404182	COMPUTER NETWORKS	PP	70	28	21	29	50	P
404183	MICROWAVE ENGINEERING	PP	70	28	14	34	48	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	23	40	63	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	17	53	70	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 464/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323031 GAIKWAD RUTUJA SANTOSH NALINI ,71637973C ,MESP ,B120323031

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	07	31	--	F
404182	COMPUTER NETWORKS	PP	70	28	16	28	44	P
404183	MICROWAVE ENGINEERING	PP	70	28	13	29	42	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	14	35	49	P
404185C	PLCS AND AUTOMATION	PP	70	28	11	28	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			29	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			33	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			25	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = --/750

B120323032 GAMBHIRE RITESH ANIL SATYASHILA ,71637974M ,MESP ,B120323032

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	19	48	67	P
404182	COMPUTER NETWORKS	PP	70	28	24	36	60	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	42	64	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	23	51	74	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	16	51	67	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			33	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			22	P
404188	PROJECT PHASE I	OR	50	20			34	P

FIRST SEM TOTAL = 488/750

B120323053 KADAM SNEHA SURESH SUVARNA ,71637985G ,MESP ,B120323053

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	42	60	P
404182	COMPUTER NETWORKS	PP	70	28	26	40	66	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	42	59	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	27	48	75	P
404185C	PLCS AND AUTOMATION	PP	70	28	24	51	75	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			44	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 533/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323055 KALE SWATI DATTATRAYA SUVARNA ,71637987C ,MESP ,B120323055

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	46	63	P
404182	COMPUTER NETWORKS	PP	70	28	22	41	63	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	59	76	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	21	52	73	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	16	49	65	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			32	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			24	P
404188	PROJECT PHASE I	OR	50	20			37	P

FIRST SEM TOTAL = 511/750

B120323059 KHAN SOHAIL DILDAR RAZIYA ,71637991M ,MESP ,B120323059

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	46	62	P
404182	COMPUTER NETWORKS	PP	70	28	19	39	58	P
404183	MICROWAVE ENGINEERING	PP	70	28	10	51	61	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	39	61	P
404185C	PLCS AND AUTOMATION	PP	70	28	27	38	65	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 488/750

B120323063 KHOT PUJA RAMCHANDRA MAYA ,71637992K ,MESP ,B120323063

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	41	57	P
404182	COMPUTER NETWORKS	PP	70	28	21	45	66	P
404183	MICROWAVE ENGINEERING	PP	70	28	18	59	77	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	29	35	64	P
404185C	PLCS AND AUTOMATION	PP	70	28	27	59	86	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			44	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 555/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323068 LANDE ANKITA ASHOK SUVARNA ,71637997L ,MESP ,B120323068

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	54	69	P
404182	COMPUTER NETWORKS	PP	70	28	20	48	68	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	62	79	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	27	49	76	P
404185C	PLCS AND AUTOMATION	PP	70	28	22	54	76	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			43	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 571/750

B120323069 MAHADIK SONAL SUDHIR MADHURI ,71637998J ,MESP ,B120323069

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	42	59	P
404182	COMPUTER NETWORKS	PP	70	28	23	40	63	P
404183	MICROWAVE ENGINEERING	PP	70	28	16	57	73	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	23	56	79	P
404185C	PLCS AND AUTOMATION	PP	70	28	25	41	66	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = 539/750

B120323074 MORE SHRUTI SHANKAR NALINI ,71638003L ,MESP ,B120323074

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	34	50	P
404182	COMPUTER NETWORKS	PP	70	28	22	25	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	14	42	56	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	18	39	57	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	29	52	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323080 OVHAL PRIYANKA MARUTI VIDYA ,71638007C ,MESP ,B120323080

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	22	48	70	P
404182	COMPUTER NETWORKS	PP	70	28	25	38	63	P
404183	MICROWAVE ENGINEERING	PP	70	28	16	63	79	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	21	50	71	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	23	51	74	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = 560/750

B120323081 PAKHARSANGAVE ANJALI ARJUN SUVARNA ,71638008M ,MESP ,B120323081

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	52	70	P
404182	COMPUTER NETWORKS	PP	70	28	22	38	60	P
404183	MICROWAVE ENGINEERING	PP	70	28	19	57	76	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	20	47	67	P
404185C	PLCS AND AUTOMATION	PP	70	28	28	37	65	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 530/750

B120323083 PATIL DEEPALI RAJENDRA SUVARNA ,71638010C ,MESP ,B120323083

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	52	69	P
404182	COMPUTER NETWORKS	PP	70	28	23	28	51	P
404183	MICROWAVE ENGINEERING	PP	70	28	21	51	72	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	58	80	P
404185C	PLCS AND AUTOMATION	PP	70	28	21	33	54	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 526/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323084 PATIL NANDAN DAYANAND JAYASHRI ,71638012K ,MESP ,B120323084

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	31	47	P
404182	COMPUTER NETWORKS	PP	70	28	20	28	48	P
404183	MICROWAVE ENGINEERING	PP	70	28	18	35	53	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	25	59	84	P
404185C	PLCS AND AUTOMATION	PP	70	28	20	48	68	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			43	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			34	P

FIRST SEM TOTAL = 499/750

B120323088 PORE AMRUTA ANANT ANITA ,71638013H ,MESP ,B120323088

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	36	51	P
404182	COMPUTER NETWORKS	PP	70	28	15	36	51	P
404183	MICROWAVE ENGINEERING	PP	70	28	16	57	73	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	25	54	79	P
404185C	PLCS AND AUTOMATION	PP	70	28	25	54	79	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 524/750

B120323089 RAKH YOGESH ABHIMAN MUKTA ,71638014F ,MESP ,B120323089

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	04	--	F
404182	COMPUTER NETWORKS	PP	70	28	20	12	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	11	09	--	F
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	23	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	13	15	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			43	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323111 TORANE MAHESH JAGDISH SANTOSHI ,71638026K ,MESP ,B120323111

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	31	48	P
404182	COMPUTER NETWORKS	PP	70	28	20	38	58	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	47	69	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	16	35	51	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	36	59	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			33	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			35	P

FIRST SEM TOTAL = 460/750

B120323004 AUTI KAJAL DATTATRAY NIRMALA ,71637957M ,MESP ,B120323004

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	34	50	P
404182	COMPUTER NETWORKS	PP	70	28	20	35	55	P
404183	MICROWAVE ENGINEERING	PP	70	28	26	37	63	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	43	65	P
404185C	PLCS AND AUTOMATION	PP	70	28	25	35	60	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			25	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 478/750

B120323016 BORSE MADHURI BALU PUSHPA ,71637963F ,MESP ,B120323016

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	45	58	P
404182	COMPUTER NETWORKS	PP	70	28	19	32	51	P
404183	MICROWAVE ENGINEERING	PP	70	28	20	42	62	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	23	55	78	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	45	68	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 493/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323023 DESHMANE ANKITA SUNIL MANGAL ,71637965B ,MESP ,B120323023

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	33	48	P
404182	COMPUTER NETWORKS	PP	70	28	13	30	43	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	33	50	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	20	45	65	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	19	40	59	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 457/750

B120323025 DESHPANDE DEEPAK RAJENDRA PRANJALA ,71637966L ,MESP ,B120323025

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	29	41	P
404182	COMPUTER NETWORKS	PP	70	28	19	27	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	20	39	59	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	26	44	70	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	19	48	67	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			39	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = --/750

B120323027 DHARWADKAR SHREYA SHRIDHAR SHRUTI ,71637968G ,MESP ,B120323027

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	32	46	P
404182	COMPUTER NETWORKS	PP	70	28	27	32	59	P
404183	MICROWAVE ENGINEERING	PP	70	28	20	36	56	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	25	36	61	P
404185C	PLCS AND AUTOMATION	PP	70	28	25	37	62	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 479/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323028 DHAVALE KAJAL BANDU HEMA ,71637970J ,MESP ,B120323028

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	41	53	P
404182	COMPUTER NETWORKS	PP	70	28	22	33	55	P
404183	MICROWAVE ENGINEERING	PP	70	28	21	37	58	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	18	45	63	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	18	42	60	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 471/750

B120323037 GOGAWALE SHRUTI RAMESH SHUBHADA ,71637977F ,MESP ,B120323037

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	07	20	--	F
404182	COMPUTER NETWORKS	PP	70	28	12	31	43	P
404183	MICROWAVE ENGINEERING	PP	70	28	12	20	--	F
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	10	33	43	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	07	32	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			32	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			37	P

FIRST SEM TOTAL = --/750

B120323049 JADHAV ROHIT SANJAY JYOTSNA ,71637983L ,MESP ,B120323049

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	19	39	58	P
404182	COMPUTER NETWORKS	PP	70	28	23	30	53	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	49	64	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	26	45	71	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	39	62	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			35	P

FIRST SEM TOTAL = 486/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323058 KAVADE SNEHAL JOTIRAM HEMALATA ,71637989K ,MESP ,B120323058

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	43	58	P
404182	COMPUTER NETWORKS	PP	70	28	15	40	55	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	AA	--	F
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	17	44	61	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	10	09	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = --/750

B120323108 THIGALE TRUPTI ASHOK UJWALA ,71638023E ,MESP ,B120323108

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	37	53	P
404182	COMPUTER NETWORKS	PP	70	28	21	35	56	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	44	61	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	22	33	55	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	20	35	55	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			41	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 477/750

B120323092 SALUNKE TANAYA SUNIL VAISHALI ,71638017L ,MESP ,B120323092

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	33	46	P
404182	COMPUTER NETWORKS	PP	70	28	21	31	52	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	45	62	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	15	30	45	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	16	37	53	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			24	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 438/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323001 ADALE POOJA ASHOK SUJATA ,71538311G ,MESP ,B120323001

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	34	48	P
404182	COMPUTER NETWORKS	PP	70	28	21	29	50	P
404183	MICROWAVE ENGINEERING	PP	70	28	23	45	68	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	25	49	74	P
404185C	PLCS AND AUTOMATION	PP	70	28	21	41	62	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			34	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 488/750

B120323056 KAMBLE MONICA MACHHINDRA TRUPTI ,71453726J ,MESP ,B120323056

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	19	--	F
404182	COMPUTER NETWORKS	PP	70	28	14	34	48	P
404183	MICROWAVE ENGINEERING	PP	70	28	18	39	57	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	12	35	47	P
404185C	PLCS AND AUTOMATION	PP	70	28	22	43	65	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			31	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			25	P
404188	PROJECT PHASE I	OR	50	20			35	P

FIRST SEM TOTAL = --/750

B120323005 AWADE ANIRUDH NAGORAO MEENA ,71538326E ,MESP ,B120323005

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	22	41	63	P
404182	COMPUTER NETWORKS	PP	70	28	17	42	59	P
404183	MICROWAVE ENGINEERING	PP	70	28	19	36	55	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	18	46	64	P
404185C	PLCS AND AUTOMATION	PP	70	28	24	42	66	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			33	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = 498/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323015 BHOSALE VARSHA RAJENDRA SUVARNA ,71538352D ,MESP ,B120323015

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	38	54	P
404182	COMPUTER NETWORKS	PP	70	28	13	33	46	P
404183	MICROWAVE ENGINEERING	PP	70	28	13	40	53	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	16	45	61	P
404185C	PLCS AND AUTOMATION	PP	70	28	22	39	61	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			34	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			28	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 454/750

B120323013 BHASALE SIDDHESH MUKESH MEENA ,71538346K ,MESP ,B120323013

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	37	55	P
404182	COMPUTER NETWORKS	PP	70	28	18	36	54	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	33	50	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	15	44	59	P
404185C	PLCS AND AUTOMATION	PP	70	28	22	35	57	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			43	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			43	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 482/750

B120323019 CHOPKAR ASHISH PRABHAKAR JYOTI ,71538379F ,MESP ,B120323019

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	40	55	P
404182	COMPUTER NETWORKS	PP	70	28	20	44	64	P
404183	MICROWAVE ENGINEERING	PP	70	28	20	42	62	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	50	72	P
404185C	PLCS AND AUTOMATION	PP	70	28	25	35	60	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = 506/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323020 DADWANI TEHSEEN SIRAJ SAMIRA ,71538381H ,MESP ,B120323020

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	08	46	54	P
404182	COMPUTER NETWORKS	PP	70	28	09	43	52	P
404183	MICROWAVE ENGINEERING	PP	70	28	13	34	47	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	40	62	P
404185C	PLCS AND AUTOMATION	PP	70	28	21	33	54	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			45	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			43	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 477/750

B120323022 DESAI VINAYAK ALIAS ANAND VILASRAO VASANTI ,71538388E ,MESP ,B120323022

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	34	45	P
404182	COMPUTER NETWORKS	PP	70	28	11	35	46	P
404183	MICROWAVE ENGINEERING	PP	70	28	16	29	45	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	20	39	59	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	19	40	59	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 437/750

B120323006 B TEJSHREE SANGITA ,71538328M ,MESP ,B120323006

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	19	47	66	P
404182	COMPUTER NETWORKS	PP	70	28	22	45	67	P
404183	MICROWAVE ENGINEERING	PP	70	28	19	37	56	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	19	50	69	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	37	60	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			45	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 522/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323009 BARASKAR VAIBHAV PADMAKAR MANGAL ,71538337L ,MESP ,B120323009

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	33	50	P
404182	COMPUTER NETWORKS	PP	70	28	18	19	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	16	30	46	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	22	31	53	P
404185C	PLCS AND AUTOMATION	PP	70	28	16	38	54	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = --/750

B120323018 CHAUDHARI MUGDHA JAYANT SANJIVANI ,71538367B ,MESP ,B120323018

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	31	44	P
404182	COMPUTER NETWORKS	PP	70	28	13	27	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	15	30	45	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	10	38	48	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	15	33	48	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = --/750

B120323024 DESHMUKH SAGAR DATTATRAY CHARUSHILA ,71538391E ,MESP ,B120323024

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	32	44	P
404182	COMPUTER NETWORKS	PP	70	28	13	16	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	08	30	--	F
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	15	28	43	P
404185C	PLCS AND AUTOMATION	PP	70	28	06	35	41	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			32	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			42	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323033 GAVHAD KARAN SANJAY SANGITA ,71538423G ,MESP ,B120323033

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	39	53	P
404182	COMPUTER NETWORKS	PP	70	28	20	38	58	P
404183	MICROWAVE ENGINEERING	PP	70	28	23	42	65	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	24	47	71	P
404185C	PLCS AND AUTOMATION	PP	70	28	30	35	65	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			07	F
404188	PROJECT PHASE I	OR	50	20			AA	F

FIRST SEM TOTAL = --/750

B120323034 GAWANDE RASHMI RAMRAO SUNITA ,71538425C ,MESP ,B120323034

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	22	39	61	P
404182	COMPUTER NETWORKS	PP	70	28	25	64	89	P
404183	MICROWAVE ENGINEERING	PP	70	28	26	48	74	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	26	54	80	P
404185C	PLCS AND AUTOMATION	PP	70	28	26	40	66	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			43	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			43	P
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = 583/750

B120323036 GHAG SHALMALEE RAJESH RAVEENA ,71538428H ,MESP ,B120323036

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	20	41	61	P
404182	COMPUTER NETWORKS	PP	70	28	22	38	60	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	40	62	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	28	45	73	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	20	47	67	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			45	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			41	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = 538/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323062 KHOLE ARUNDHATI ARUNKUMAR ANUPAMA ,71538499G ,MESP ,B120323062

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	AA	40	40	P
404182	COMPUTER NETWORKS	PP	70	28	18	31	49	P
404183	MICROWAVE ENGINEERING	PP	70	28	09	51	60	P
404184C	SOFTWARE DEFINED RADIO	PP	70	28	24	51	75	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	14	36	50	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			44	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			44	P
404188	PROJECT PHASE I	OR	50	20			44	P

FIRST SEM TOTAL = 494/750

B120323007 BACHHAV DEEPIKA DADAJI SARALA ,71538330C ,MESP ,B120323007

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	23	32	55	P
404182	COMPUTER NETWORKS	PP	70	28	22	37	59	P
404183	MICROWAVE ENGINEERING	PP	70	28	25	39	64	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	25	46	71	P
404185C	PLCS AND AUTOMATION	PP	70	28	25	43	68	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			43	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 523/750

B120323011 BHAGAT MANALI MANOJ KANCHAN ,71538340L ,MESP ,B120323011

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	33	44	P
404182	COMPUTER NETWORKS	PP	70	28	20	29	49	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	37	52	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	12	35	47	P
404185C	PLCS AND AUTOMATION	PP	70	28	21	28	49	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			27	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			28	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 415/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323040 GORE PRACHI PRAKASH RAJASHREE ,71538435L ,MESP ,B120323040

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	36	48	P
404182	COMPUTER NETWORKS	PP	70	28	22	42	64	P
404183	MICROWAVE ENGINEERING	PP	70	28	23	28	51	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	22	39	61	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	32	55	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			32	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			28	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = 465/750

B120323044 GUPTA PRERNA PRADIP KHUSHBALA ,71538441E ,MESP ,B120323044

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	22	37	59	P
404182	COMPUTER NETWORKS	PP	70	28	15	44	59	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	40	62	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	19	47	66	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	20	51	71	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			31	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			25	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			36	P

FIRST SEM TOTAL = 487/750

B120323038 GONJARI ANUJA MAHESH MINAKSHI ,71538434B ,MESP ,B120323038

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	35	52	P
404182	COMPUTER NETWORKS	PP	70	28	24	42	66	P
404183	MICROWAVE ENGINEERING	PP	70	28	25	45	70	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	26	47	73	P
404185C	PLCS AND AUTOMATION	PP	70	28	26	38	64	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 520/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323041 GUGALE TEJAS LALITKUMAR TILOTTAMA ,71538439C ,MESP ,B120323041

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	16	--	F
404182	COMPUTER NETWORKS	PP	70	28	15	37	52	P
404183	MICROWAVE ENGINEERING	PP	70	28	23	43	66	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	22	45	67	P
404185C	PLCS AND AUTOMATION	PP	70	28	20	39	59	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = --/750

B120323052 KADAM PRANJALI VINOD VIMAL ,71538471G ,MESP ,B120323052

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	20	46	66	P
404182	COMPUTER NETWORKS	PP	70	28	24	45	69	P
404183	MICROWAVE ENGINEERING	PP	70	28	20	61	81	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	27	47	74	P
404185C	PLCS AND AUTOMATION	PP	70	28	27	46	73	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 561/750

B120323065 KSHIRSAGAR DIPANJALI RAVINDRA SUVARNA ,71538509H ,MESP ,B120323065

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	29	45	P
404182	COMPUTER NETWORKS	PP	70	28	18	49	67	P
404183	MICROWAVE ENGINEERING	PP	70	28	12	55	67	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	27	48	75	P
404185C	PLCS AND AUTOMATION	PP	70	28	28	31	59	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			44	P

FIRST SEM TOTAL = 499/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323082 PANDKAR SHUBHAM RAJAN SHUBHADA ,71538562D ,MESP ,B120323082

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	19	49	68	P
404182	COMPUTER NETWORKS	PP	70	28	14	28	42	P
404183	MICROWAVE ENGINEERING	PP	70	28	14	55	69	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	21	46	67	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	20	48	68	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			43	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = 515/750

B120323085 PATIL PRASHANT NANABHAU SANGITA ,71538578L ,MESP ,B120323085

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	31	46	P
404182	COMPUTER NETWORKS	PP	70	28	15	29	44	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	44	59	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	15	36	51	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	14	44	58	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			25	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			30	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 430/750

B120323048 JADHAV PRAJAKTA ASHOK USHA ,71538451B ,MESP ,B120323048

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	45	61	P
404182	COMPUTER NETWORKS	PP	70	28	21	38	59	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	56	78	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	24	45	69	P
404185C	PLCS AND AUTOMATION	PP	70	28	18	36	54	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			32	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			37	P

FIRST SEM TOTAL = 493/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323050 JIBHAKATE PRANJALI RAMESH MANISHA ,71538466L ,MESP ,B120323050

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	31	48	P
404182	COMPUTER NETWORKS	PP	70	28	26	42	68	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	55	77	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	30	51	81	P
404185C	PLCS AND AUTOMATION	PP	70	28	27	36	63	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 537/750

B120323079 NIKAM SHUBHANGI NAVANATH ANITA ,71538552G ,MESP ,B120323079

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	39	55	P
404182	COMPUTER NETWORKS	PP	70	28	22	39	61	P
404183	MICROWAVE ENGINEERING	PP	70	28	19	59	78	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	23	60	83	P
404185C	PLCS AND AUTOMATION	PP	70	28	25	38	63	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			42	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 544/750

B120323086 PHADKE SOMNATH ANKUSH USHA ,71538587K ,MESP ,B120323086

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	33	51	P
404182	COMPUTER NETWORKS	PP	70	28	20	43	63	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	57	74	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	25	54	79	P
404185C	PLCS AND AUTOMATION	PP	70	28	30	45	75	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			45	P

FIRST SEM TOTAL = 553/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323029 GADAKH SAYALI ANNASAHEB SMITA ,71538411C ,MESP ,B120323029

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	46	64	P
404182	COMPUTER NETWORKS	PP	70	28	25	35	60	P
404183	MICROWAVE ENGINEERING	PP	70	28	24	46	70	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	26	43	69	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	25	51	76	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			43	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			43	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			43	P
404188	PROJECT PHASE I	OR	50	20			44	P

FIRST SEM TOTAL = 556/750

B120323046 JADHAV DIMPAL ASHOK MANGALA ,71538448B ,MESP ,B120323046

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	07	45	52	P
404182	COMPUTER NETWORKS	PP	70	28	05	44	49	P
404183	MICROWAVE ENGINEERING	PP	70	28	18	50	68	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	25	52	77	P
404185C	PLCS AND AUTOMATION	PP	70	28	26	39	65	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			25	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			07	F
404188	PROJECT PHASE I	OR	50	20			41	P

FIRST SEM TOTAL = --/750

B120323061 KHEDEKAR PUNAM LAXMAN LALITA ,71538498J ,MESP ,B120323061

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	39	54	P
404182	COMPUTER NETWORKS	PP	70	28	16	31	47	P
404183	MICROWAVE ENGINEERING	PP	70	28	19	40	59	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	24	39	63	P
404185C	PLCS AND AUTOMATION	PP	70	28	18	24	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			43	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			39	P
404188	PROJECT PHASE I	OR	50	20			37	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323064 KOLEKAR NAYAN SHANTINATH VAISHALI ,71538502L ,MESP ,B120323064

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	57	74	P
404182	COMPUTER NETWORKS	PP	70	28	23	52	75	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	56	78	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	29	48	77	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	19	48	67	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			34	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			39	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = 566/750

B120323067 KURHADE AKSHAY GANPAT SANGITA ,71538512H ,MESP ,B120323067

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	48	64	P
404182	COMPUTER NETWORKS	PP	70	28	21	41	62	P
404183	MICROWAVE ENGINEERING	PP	70	28	22	48	70	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	25	43	68	P
404185C	PLCS AND AUTOMATION	PP	70	28	27	60	87	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			34	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			45	P

FIRST SEM TOTAL = 549/750

B120323070 MAHAJAN CHETAN RAGHUNATH PRATIBHA ,71538516L ,MESP ,B120323070

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	41	54	P
404182	COMPUTER NETWORKS	PP	70	28	05	29	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	16	46	62	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	19	39	58	P
404185C	PLCS AND AUTOMATION	PP	70	28	18	28	46	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			28	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			39	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323076 NALEWAD ANKUSH ANANTA MADALASA ,71538543H ,MESP ,B120323076

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	43	58	P
404182	COMPUTER NETWORKS	PP	70	28	12	38	50	P
404183	MICROWAVE ENGINEERING	PP	70	28	15	28	43	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	15	46	61	P
404185C	PLCS AND AUTOMATION	PP	70	28	23	41	64	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			34	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 462/750

B120323096 SAWALE MUGHADHA NAGESH SUSHAMA ,71538618C ,MESP ,B120323096

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	36	52	P
404182	COMPUTER NETWORKS	PP	70	28	22	30	52	P
404183	MICROWAVE ENGINEERING	PP	70	28	19	44	63	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	27	52	79	P
404185C	PLCS AND AUTOMATION	PP	70	28	20	31	51	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 499/750

B120323102 SNEHA PAUL THOMAS SALLY ,71538656F ,MESP ,B120323102

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	19	29	48	P
404182	COMPUTER NETWORKS	PP	70	28	22	40	62	P
404183	MICROWAVE ENGINEERING	PP	70	28	25	51	76	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	29	58	87	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	26	57	83	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			45	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			45	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			43	P
404188	PROJECT PHASE I	OR	50	20			43	P

FIRST SEM TOTAL = 572/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323105 SURE SHUBHAM SANJEEV SADHANA ,71538663J ,MESP ,B120323105

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	19	44	63	P
404182	COMPUTER NETWORKS	PP	70	28	18	35	53	P
404183	MICROWAVE ENGINEERING	PP	70	28	18	49	67	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	26	38	64	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	23	40	63	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			43	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			42	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = 518/750

B120323107 TANWADE ONKAR SUNIL SUVARNA ,71538668K ,MESP ,B120323107

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	14	33	47	P
404182	COMPUTER NETWORKS	PP	70	28	16	37	53	P
404183	MICROWAVE ENGINEERING	PP	70	28	26	33	59	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	24	39	63	P
404185C	PLCS AND AUTOMATION	PP	70	28	21	38	59	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			42	P
404188	PROJECT PHASE I	OR	50	20			44	P

FIRST SEM TOTAL = 487/750

B120323117 WAREKAR TEJASWINI MANIKRAO URMILA ,71538693L ,MESP ,B120323117

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	27	50	77	P
404182	COMPUTER NETWORKS	PP	70	28	27	35	62	P
404183	MICROWAVE ENGINEERING	PP	70	28	25	64	89	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	20	38	58	P
404185C	PLCS AND AUTOMATION	PP	70	28	27	51	78	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			45	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			45	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = 578/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323119 YANNAM ROHIT NARAYAN VANITA ,71538695G ,MESP ,B120323119

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	28	43	P
404182	COMPUTER NETWORKS	PP	70	28	13	26	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	18	34	52	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	18	38	56	P
404185C	PLCS AND AUTOMATION	PP	70	28	21	29	50	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			37	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323094 SATBHAI AKHIL BHARATRAO BHAVANA ,71538617E ,MESP ,B120323094

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	19	--	F
404182	COMPUTER NETWORKS	PP	70	28	18	24	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	18	46	64	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	22	40	62	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	13	43	56	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			41	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			32	P
404188	PROJECT PHASE I	OR	50	20			40	P

FIRST SEM TOTAL = --/750

B120323098 SHAH ADITI SUNIL SONALI ,71538621C ,MESP ,B120323098

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	16	36	52	P
404182	COMPUTER NETWORKS	PP	70	28	20	28	48	P
404183	MICROWAVE ENGINEERING	PP	70	28	27	32	59	P
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	15	29	44	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	17	41	58	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			33	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			40	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = 454/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323106 TAMBE POOJA MILIND VIDYA ,71538666C ,MESP ,B120323106

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	34	52	P
404182	COMPUTER NETWORKS	PP	70	28	22	37	59	P
404183	MICROWAVE ENGINEERING	PP	70	28	25	48	73	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	24	40	64	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	23	34	57	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			45	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			45	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			44	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			42	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = 523/750

B120323110 TINGRE RUTUJA SATISH ASHADEVI ,71538674D ,MESP ,B120323110

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	40	58	P
404182	COMPUTER NETWORKS	PP	70	28	17	39	56	P
404183	MICROWAVE ENGINEERING	PP	70	28	23	56	79	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	16	41	57	P
404185C	PLCS AND AUTOMATION	PP	70	28	22	28	50	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			35	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			38	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = 483/750

B120323104 SONAR KANCHAN PRASAD PALLAVI ,71538658B ,MESP ,B120323104

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	20	49	69	P
404182	COMPUTER NETWORKS	PP	70	28	16	33	49	P
404183	MICROWAVE ENGINEERING	PP	70	28	19	46	65	P
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	20	38	58	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	22	39	61	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			39	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			35	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			37	P
404188	PROJECT PHASE I	OR	50	20			42	P

FIRST SEM TOTAL = 493/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323128 JADHAO NIKUL SUDHAKAR KANTA ,71504670F ,MESP ,B120323128

SEM.:1

										SEM.:2								
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	35	52	P	C	404189	MOBILE COMMUNICATION	PP	70	28	15	34	49	P	C
404182	COMPUTER NETWORKS	PP	70	28	15	33	48	P	C	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	20	33	53	P	C
404183	MICROWAVE ENGINEERING	PP	70	28	14	42	56	P	C	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	12	41	53	P	
404184C	SOFTWARE DEFINED RADIO	PP	70	28	08	36	44	P	C	404192D	WIRELESS NETWORKS	PP	70	28	19	48	67	P	C
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	21	38	59	P	C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			20	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			43	P	C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			22	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P	C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			34	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P	C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			32	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			34	P	C	404195	PROJECT PHASE II	TW	100	40			86	P	C
404188	PROJECT PHASE I	OR	50	20			38	P	C	404195	PROJECT PHASE II	PR	50	20			42	P	C

GRAND TOTAL = 907/1500 , RESULT:FIRST CLASS

B120323090 RAMTEKE AKSHAY DADARAO VANDANA ,71504692G ,MESP ,B120323090

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	33	46 P
404182	COMPUTER NETWORKS	PP	70	28	12	23	-- F
404183	MICROWAVE ENGINEERING	PP	70	28	16	42	58 P
404184C	SOFTWARE DEFINED RADIO	PP	70	28	22	46	68 P
404185C	PLCS AND AUTOMATION	PP	70	28	24	48	72 P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40 P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38 P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			40 P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			42 P
404188	PROJECT PHASE I	OR	50	20			40 P

FIRST SEM TOTAL = --/750

B120323129 KADAM NIKHIL DASHRATH JAYSHREE ,71412347B ,MESP ,B120323129

SEM.:1

										SEM.:2								
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	29	47	P	C	404189	MOBILE COMMUNICATION	PP	70	28	17	30	47	P	C
404182	COMPUTER NETWORKS	PP	70	28	12	31	43	P	C	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	17	29	46	P	C
404183	MICROWAVE ENGINEERING	PP	70	28	22	33	55	P		404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	02	29	--	F	
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	17	36	53	P		404192D	WIRELESS NETWORKS	PP	70	28	06	34$	40	P	C
404185C	PLCS AND AUTOMATION	PP	70	28	13	41	54	P	C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			24	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			38	P	C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			27	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P	C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			30	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			42	P	C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			28	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P	C	404195	PROJECT PHASE II	TW	100	40			75	P	C
404188	PROJECT PHASE I	OR	50	20			35	P	C	404195	PROJECT PHASE II	PR	50	20			35	P	C

GRAND TOTAL = --/1500 , RESULT:FAILS [$ 0.1]

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323131 PANDALAI ADITYA NARAYANAN PREETHA ,71412448G ,MESP ,B120323131

SEM.:1

										SEM.:2								
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	12	31	43	P	C	404189	MOBILE COMMUNICATION	PP	70	28	14	36	50	P	C
404182	COMPUTER NETWORKS	PP	70	28	15	34	49	P		404190	BROADBAND COMMUNICATION SYS.	PP	70	28	23	28	51	P	C
404183	MICROWAVE ENGINEERING	PP	70	28	07	33	40	P	C	404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	13	31	44	P	C
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	20	28	48	P		404192B	NANO ELECTRONICS & MEMS	PP	70	28	19	34	53	P	C
404185C	PLCS AND AUTOMATION	PP	70	28	22	33	55	P	C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			34	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P	C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			34	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P	C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			37	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			37	P	C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			34	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			39	P	C	404195	PROJECT PHASE II	TW	100	40			80	P	C
404188	PROJECT PHASE I	OR	50	20			41	P	C	404195	PROJECT PHASE II	PR	50	20			40	P	C

GRAND TOTAL = 887/1500 , RESULT:HIGHER SECOND CLASS

B120323115 VIVEK PARASHURAM GADIWADDAR MEENA ,71504705B ,MESP ,B120323115

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	21	--	F
404182	COMPUTER NETWORKS	PP	70	28	13	18	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	17	14	--	F
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	08	23	--	F
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	12	24	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			41	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			40	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			30	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			39	P

FIRST SEM TOTAL = --/750

B120323122 BHUREWAR RAUNAK RAJENDRA SUNITA BHUREWAR ,71312338K ,MESP ,B120323122

SEM.:1

										SEM.:2								
404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	13	29	42	P	C	404189	MOBILE COMMUNICATION	PP	70	28	07	35	42	P	C
404182	COMPUTER NETWORKS	PP	70	28	14	28$	42	P	C	404190	BROADBAND COMMUNICATION SYS.	PP	70	28	18	28$	46	P	C
404183	MICROWAVE ENGINEERING	PP	70	28	27	28	55	P		404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	10	30$	40	P	C
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	10	30$	40	P	C	404192D	WIRELESS NETWORKS	PP	70	28	09	40	49	P	C
404185C	PLCS AND AUTOMATION	PP	70	28	16	36	52	P	C	404193	LAB PRACTICE III(MC & BCS)	TW	50	20			20	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P	C	404193	LAB PRACTICE III(MC & BCS)	OR	50	20			22	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			25	P	C	404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			32	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			22	P	C	404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			28	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			20	P	C	404195	PROJECT PHASE II	TW	100	40			75	P	C
404188	PROJECT PHASE I	OR	50	20			31	P	C	404195	PROJECT PHASE II	PR	50	20			34	P	C

GRAND TOTAL = 753/1500 , RESULT:SECOND CLASS [$ 0.1]

RESULT RESERVED FOR BACKLOGS.

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323017 BURUD TRUPTI VASANT LATA ,71312347J ,MESP ,B120323017

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	15	36	51	P
404182	COMPUTER NETWORKS	PP	70	28	15	18	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	09	13	--	F
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	18	35	53	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	14	30	44	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			36	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			31	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			28	P
404188	PROJECT PHASE I	OR	50	20			33	P

FIRST SEM TOTAL = --/750

B120323060 KHARAT SUSHANT SANJAY REKHA ,71312471H ,MESP ,B120323060

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	18	18	--	F
404182	COMPUTER NETWORKS	PP	70	28	11	35	46	P
404183	MICROWAVE ENGINEERING	PP	70	28	12	23	--	F
404184B	EMBEDDED SYSTEMS & RTOS	PP	70	28	20	30	50	P
404185C	PLCS AND AUTOMATION	PP	70	28	18	29	47	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			37	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			36	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			29	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			35	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = --/750

B120323077 NAMAGAVALI NIRALI SUNIL MADHVI ,71312531E ,MESP ,B120323077

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	06	07	--	F
404182	COMPUTER NETWORKS	PP	70	28	10	18	--	F
404183	MICROWAVE ENGINEERING	PP	70	28	09	41	50	P
404184C	SOFTWARE DEFINED RADIO	PP	70	28	13	28	41	P
404185C	PLCS AND AUTOMATION	PP	70	28	02	23	--	F
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			40	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			41	P
404188	PROJECT PHASE I	OR	50	20			35	P

FIRST SEM TOTAL = --/750

NOTE: FIRST LINE : SEAT NO., NAME OF THE CANDIDATE, MOTHER, PERMANENT REG. NO., PREVIOUS SEAT NO., COLLEGE, SEAT NO.
OTHER LINES: HEAD OF PASSING, MAX. MARKS, MIN.PASS MARKS, INT. MARKS, TH. MARKS, TOTAL MARKS OBTAINED, P/F:PASS/FAIL, C:PREVIOUS CARRY OVER

B120323095 SATPUTE SAURABH PRADEEP SANGITA ,71312598F ,MESP ,B120323095

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	11	12	--	F
404182	COMPUTER NETWORKS	PP	70	28	14	31	45	P
404183	MICROWAVE ENGINEERING	PP	70	28	17	08	--	F
404184A	DIGITAL IMAGE PROCESSING	PP	70	28	18	45	63	P
404185D	ARTIFICIAL INTELLIGENCE	PP	70	28	23	50	73	P
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			42	P
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			38	P
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			39	P
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			36	P
404188	PROJECT PHASE I	OR	50	20			38	P

FIRST SEM TOTAL = --/750

B120323127 INGLE PARIXIT SURESH SUNEETA ,71110257M ,MESP ,B120323127

SEM.:1

404181	VLSI DESIGN & TECHNOLOGY	PP	70	28	17	37	54	P	C
404182	COMPUTER NETWORKS	PP	70	28	11	30	41	P	C
404183	MICROWAVE ENGINEERING	PP	70	28	08	38	46	P	
404184C	SOFTWARE DEFINED RADIO	PP	70	28	08	39	47	P	C
404185C	PLCS AND AUTOMATION	PP	70	28	19	40	59	P	C
404186	LAB PRACTICE I (CN & MWE)	TW	50	20			35	P	C
404186	LAB PRACTICE I (CN & MWE)	OR	50	20			25	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	TW	50	20			35	P	C
404187	LAB PRAC. II(VLSI &ELEC. I)	PR	50	20			25	P	C
404188	PROJECT PHASE I	OR	50	20			44	P	C

SEM.:2

404189	MOBILE COMMUNICATION	PP	70	28	13	36	49	P	C
404190	BROADBAND COMMUNICATION SYS.	PP	70	28	06	39	45	P	C
404191A	SPEECH & AUDIO SIGNAL PROC.	PP	70	28	09	38	47	P	C
404192B	NANO ELECTRONICS & MEMS	PP	70	28	25	43	68	P	C
404193	LAB PRACTICE III(MC & BCS)	TW	50	20			20	P	C
404193	LAB PRACTICE III(MC & BCS)	OR	50	20			21	P	C
404194	LAB PRAC. IV(ELECTIVE III)	TW	50	20			30	P	C
404194	LAB PRAC. IV(ELECTIVE III)	PR	50	20			28	P	C
404195	PROJECT PHASE II	TW	100	40			96	P	C
404195	PROJECT PHASE II	PR	50	20			48	P	C

GRAND TOTAL = 863/1500 , RESULT:HIGHER SECOND CLASS